

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-310US1	Application No. 10/070,091
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date February 27, 2002	Group Art Unit

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date (If Appropriate)
<i>g</i>	AA	09/473,571	12/28/1999	Wolrich et al.			
<i>g</i>	AB	09/475,614	12/30/1999	Wolrich et al.			
	AC						
	AD						
	AE						
	AF						
	AG						

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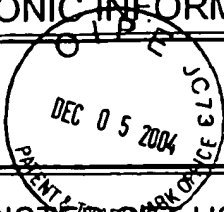
Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
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<i>g</i>	AH	WO 01/16697	03/2001	WIPO				
<i>g</i>	AI	WO 01/16698	03/2001	WIPO				
<i>g</i>	AJ	WO 01/16703	03/2001	WIPO				
<i>g</i>	AK	WO 01/16713	03/2001	WIPO				
<i>g</i>	AL	WO 01/16714	03/2001	WIPO				
<i>g</i>	AM	WO 01/16715	03/2001	WIPO				
<i>g</i>	AN	WO 01/16716	03/2001	WIPO				
<i>g</i>	AO	WO 01/16722	03/2001	WIPO				
<i>g</i>	AP	WO 01/16758	03/2001	WIPO				
<i>g</i>	AQ	WO 01/18646	03/2001	WIPO				
	AR							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
<i>g</i>	AS	Paver et al., "Register Locking in Asynchronous Processor Computer Design: VLSI Processors," ICCD '92 Proceedings, IEEE 1992 International Conference, 1992, pp. 351-355.
<i>g</i>	AT	Waldspurger et al., "Register Relocation: Flexible Contents for Multithreading," Proceedings of the 20th Annual International Symposium on Computer Architecture, 1993, pp. 120-130.
	AU	

Examiner Signature <i>[Signature]</i>	Date Considered <i>[Signature]</i>
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18  
 Stylesheet Version v18.0



Title of Invention

REGISTERED SET USED IN MULTITHREADED PARALLEL  
 PROCESSOR ARCHITECTURE

Application Number: 10/070091

Confirmation Number: 7309

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-310US1

Search string: ( 3373408 or 3478322 or 3792441 or 3913074 or 3940745 or  
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 4724521 or 4745544 or 4777587 or 4866664 or 5073864 or  
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 20040073728 or 20040073778 or 20040098496 or 20040109369 or  
 20040205747 ).pn.



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Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
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h	2	3478322	1969-11-11	Evans			
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h	4	3913074	1975-10-14	Homberg et al.			
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h	8	4400770	1983-08-23	Chan et al.			
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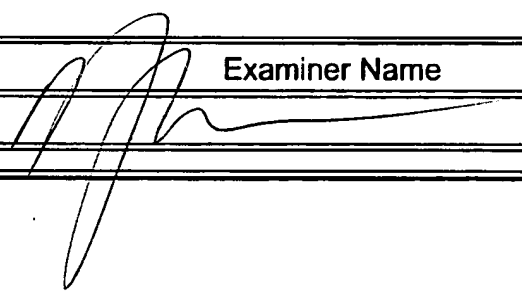

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Note: Applicant is not required to submit a paper copy of cited US Published Applications

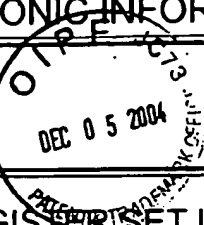
init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
<i>W</i>	1	20020053017	2002-05-02	Adiletta et al.			
<i>W</i>	2	20020056037	2002-05-09	Wolrich et al.			
<i>W</i>	3	20030041228	2003-02-27	Rosenbluth et al.			
<i>W</i>	4	20030145159	2003-07-31	Adiletta et al.			
<i>W</i>	5	20030191866	2003-10-09	Wolrich et al.			
<i>W</i>	6	20040039895	2004-02-26	Wolrich et al.			
<i>W</i>	7	20040054880	2004-03-18	Bernstein et al.			
<i>W</i>	8	20040071152	2004-04-15	Wolrich et al.			
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<i>W</i>	11	20040098496	2004-05-20	Wolrich et al.			
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Signature

	Examiner Name		Date

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Electronic Version v18  
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Title of Invention

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PROCESSOR ARCHITECTURE

Application Number: 10/070091

Confirmation Number: 7309

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-310US1

Search string: ( 5568617 or 5574922 or 5574939 or 5592622 or 5606676 or  
5613071 or 5613136 or 5623489 or 5627829 or 5630130 or  
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## US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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W	2	5574922	1996-11-12	James			
W	3	5574939	1996-11-12	Keckler et al.			
W	4	5592622	1997-01-07	Isfeld et al.			
W	5	5606676	1997-02-25	Grochowski et al.			
W	6	5613071	1997-03-18	Rankin et al.			
W	7	5613136	1997-03-18	Casavant et al.			
W	8	5623489	1997-04-22	Cotton et al.			
W	9	5627829	1997-05-06	Gleeson et al.			
W	10	5630130	1997-05-13	Perotto et al.			
W	11	5644623	1997-07-01	Gulledge			
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W	13	5659722	1997-08-19	Blaner et al.			
W	14	5680641	1997-10-21	Sidman			
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50	5659687	1997-08-19	Kim et al.

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# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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Title of Invention

**REGISTER SET USED IN MULTITHREADED PARALLEL  
 PROCESSOR ARCHITECTURE**

Application Number: 10/070091

Confirmation Number: 7309

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-310US1

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## US Patent Documents

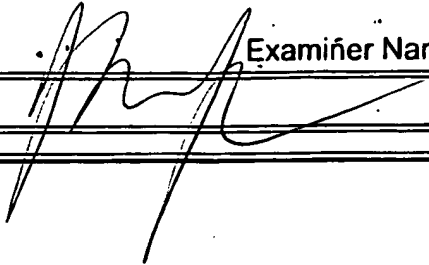
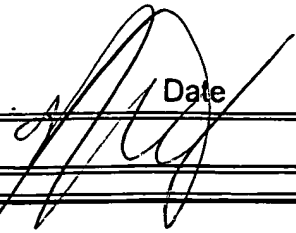
Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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h	1	5937187	1999-08-10	Kosche et al.			
h	2	5938736	1999-08-17	Muller et al.			
h	3	5940612	1999-08-17	Brady et al.			
h	4	5940866	1999-08-17	Chisholm et al.			
h	5	5946487	1999-08-31	Dangelo			
h	6	5948081	1999-09-07	Foster			
h	7	5951679	1999-09-14	Anderson et al.			
h	8	5958031	1999-09-28	Kim			
h	9	5961628	1999-10-05	Nguyen et al.			
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h	11	5978838	1999-11-02	Mohamed et al.			
h	12	5983274	1999-11-09	Hyder et al.			
h	13	5996068	1999-11-30	Dwyer III et al.			
h	14	6002881	1999-12-14	York et al.			
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✓	16	6012151	2000-01-04	Mano
✓	17	6014729	2000-01-11	Lannan et al.
✓	18	6023742	2000-02-08	Ebeling et al.
✓	19	6058168	2000-05-02	Braband
✓	20	6058465	2000-05-02	Nguyen
✓	21	6067585	2000-05-23	Hoang
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✓	23	6072781	2000-06-06	Feeney et al.
✓	24	6073215	2000-06-06	Snyder
✓	25	6076158	2000-06-13	Sites et al.
✓	26	6079008	2000-06-20	Clery III
✓	27	6079014	2000-06-20	Papworth et al.
✓	28	6085215	2000-07-04	Ramakrishnan et al.
✓	29	6085294	2000-07-04	Van Doren et al.
✓	30	6092127	2000-07-18	Tausheck
✓	31	6092158	2000-07-18	Harriman et al.
✓	32	6112016	2000-08-29	MacWilliams et al.
✓	33	6115811	2000-09-05	Steele Jr.
✓	34	6134665	2000-10-17	Klein et al.
✓	35	6141689	2000-10-31	Yasrebi
✓	36	6141765	2000-10-31	Sherman
✓	37	6144669	2000-11-07	Williams et al.
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✓	49	6009505	1999-12-28	Thayer et al.
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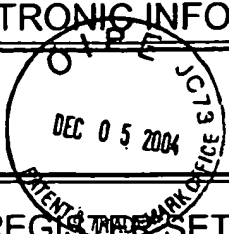
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# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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 Stylesheet Version v18.0



Title of Invention

**REGISTER SET USED IN MULTITHREADED PARALLEL  
 PROCESSOR ARCHITECTURE**

Application Number: 10/070091  
 Confirmation Number: 7309  
 First Named Applicant: Gilbert Wolrich  
 Attorney Docket Number: 10559-310US1  
 Search string: ( 6223238 or 6223279 or 6247025 or 6256713 or 6272616 or  
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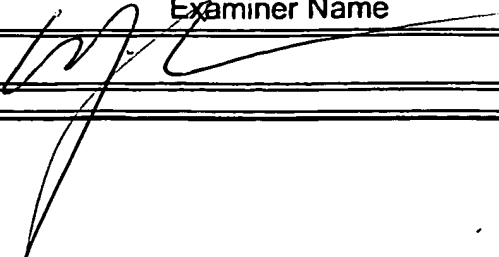
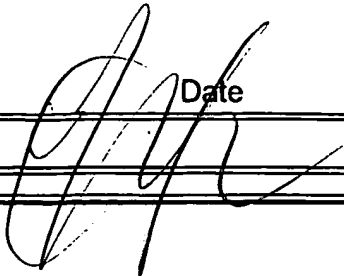
## US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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✓	2	6223279	2001-04-24	Nishimura et al.			
✓	3	6247025	2001-06-12	Bacon			
✓	4	6256713	2001-07-03	Audityan et al.			
✓	5	6272616	2001-08-07	Fernando et al.			
✓	6	6275505	2001-08-14	O Loughlin et al.			
✓	7	6279113	2001-08-21	Vaidya			
✓	8	6289011	2001-09-11	Seo et al.			
✓	9	6298370	2001-10-02	Tang et al.			
✓	10	6307789	2001-10-23	Wolrich et al.			
✓	11	6324624	2001-11-27	Wolrich et al.			
✓	12	6345334	2002-02-05	Nakagawa et al.			
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✓	14	6351808	2002-02-26	Joy et al.			
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u	21	6426940	2002-07-30	Seo et al.
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u	23	6430626	2002-08-06	Witkowski et al.
u	24	6434145	2002-08-13	Opsasnick et al.
u	25	6463072	2002-10-08	Wolrich et al.
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u	29	6577542	2003-06-10	Wolrich et al.
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u	31	6587906	2003-07-01	Wolrich et al.
u	32	6606704	2003-08-12	Adiletta et al.
u	33	6625654	2003-09-23	Wolrich et al.
u	34	6629237	2003-09-30	Wolrich et al.
u	35	6631430	2003-10-07	Wolrich et al.
u	36	6631462	2003-10-07	Wolrich et al.
u	37	6661794	2003-12-09	Wolrich et al.
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u	40	6681300	2004-01-20	Wolrich et al.
u	41	6694380	2004-02-17	Wolrich et al.
u	42	4023023	1977-05-10	Bourrez et al.
u	43	5113516	1992-05-12	Johnson
u	44	5363448	1994-11-08	Koopman Jr. et al.
u	45	5436626	1995-07-25	Fijiwara
u	46	5600812	1997-02-04	Park
u	47	5652583	1997-07-29	Kang
u	48	5717760	1998-02-10	Satterfield
u	49	4992934	1991-02-12	Portanova et al.
u	50	5450603	1995-09-12	Davies

Signature

<b>Examiner Name</b> 	<b>Date</b> 
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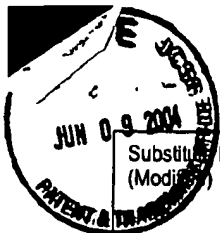
Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-310US1	Application No. <b>10/070091</b>
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date	Group Art Unit

U.S. Patent Documents							
Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
<i>h</i>	AA	5,357,617	10/18/1994	Davis et al.			
<i>h</i>	AB	5,933,627	08/03/1999	Parady			
<i>h</i>	AC	6,092,175	07/18/2000	Levy et al.			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AQ	
	AR	
	AS	
	AT	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-310US1	Application No. 10/070,091
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date February 27, 2002	Group Art Unit 2183

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
h	AA	WO 01/50679	07/12/2001	WIPO				
h	AB	WO 01/50247	07/12/2001	WIPO				
h	AC	WO 01/48619	07/05/2001	WIPO				
h	AD	WO 01/48606	07/05/2001	WIPO				
h	AE	WO 01/48599	07/05/2001	WIPO				
h	AF	WO 01/48596	07/05/2001	WIPO				
h	AG	WO 01/41530	06/14/2001	WIPO				
h	AH	WO 01/16782	03/08/2001	WIPO				
h	AI	WO 01/16770	03/08/2001	WIPO				
h	AJ	WO 01/16769	03/08/2001	WIPO				
h	AK	WO 01/16718	03/08/2001	WIPO				
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h	AM	WO 97/38372	10/16/1997	WIPO				
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h	AO	EP 0 809 180	11/26/1997	Europe				
h	AP	EP 0 745 933	12/04/1996	Europe				
h	AQ	EP 0 633 678	01/11/1995	Europe				
h	AR	EP 0 464 715	01/08/1992	Europe				
h	AS	EP 0 379 709	08/01/1990	Europe				
h	AT	59111533	06/27/1984	Japan				

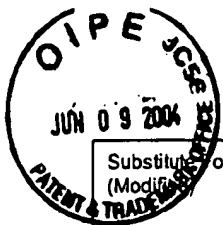
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Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
h	AU	Agarwal et al., "April: A Processor Architecture for Multiprocessing," Proceedings of the 17 <sup>th</sup> Annual International Symposium on Computer Architecture, IEEE, pp. 104-114.
h	AV	Byrd et al., "Multithread Processor Architectures," IEEE Spectrum, Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
h	AW	Chang et al., "A New Mechanism For Improving Branch Predictor Performance," IEEE, pp. 22-31 (1994).

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



Substitute Disclosure Form PTO-1449	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-310US1	Application No. 10/070001
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date February 27, 2002	Group Art Unit 2183

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**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
W	AX	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 <sup>nd</sup> ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.
W	AY	Farkas et al., "The multicluster architecture: reducing cycle time through partitioning," IEEE, vol. 30, December 1997, pp. 149-159.
W	AZ	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
W	AAA	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
W	ABB	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
W	ACC	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
W	ADD	Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482.
W	AEE	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225.
W	AFF	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21.
W	AGG	Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998.
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W	AII	Mendelson et al., "Design Alternatives of Multithreaded Architecture," <i>International Journal of Parallel Programming</i> , vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193.
W	AJJ	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998.
W	AKK	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
W	ALL	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 <sup>th</sup> Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
W	AMM	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1998.
W	ANN	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , 18 March 1999.
W	AOO	Vibhatavanijit et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359.
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